Garrett Knuf

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EDUCATION

California Institute of Technology Pasadena, CA
B.S. Electrical Engineering | 4.1/4.3 GPA Expected Jun 2025

- Relevant Coursework: Mixed-Mode IC Design, Analog Circuit Design, Digital Systems Design, Computer Architecture, Feedback and Control Systems, Embedded Systems, Signal Processing, Machine Learning, and Operating Systems

WORK EXPERIENCE

Cadence Design Systems San Jose, CA
Application Engineer Intern (Digital Design and Signoff) Jun 2024 – Aug 2024

- Executed ASIC physical design flow for high-speed digital signal processing IP block using Cadence tools (Genus, Innovus)
- Explored topologies for floorplanning, power planning, and clock tree synthesis to optimize power, performance, and area
- Analyzed timing, congestion, and routing challenges and improved overall chip performance through iterative optimization

Caltech Mixed-Mode Integrated Circuits and Systems Lab Pasadena, CA
Undergraduate Researcher Sep 2023 – Jun 2025

- Optimized digital ASIC interface to minimize microcontroller power consumption in a wearable biomedical sensor system
- Developed Nordic MCU software, implementing and debugging I2C-ASIC communication and BLE connectivity
- Identified and resolved serial interface performance issues, improving data integrity and communication reliability

Honeybee Robotics Altadena, CA
Embedded Software Engineer Intern Jun 2023 – Sep 2023

- Developed flight software in C for sample acquisition system on NASA's Dragonfly mission
- Designed and implemented state machines for mission operations with software testbenches at 100% code coverage
- Coordinated system-level design with electrical and FPGA teams to ensure alignment of design specifications

Undergraduate Researcher La Canada Flintridge, CA
NASA Jet Propulsion Laboratory, Telecommunications Architectures and Research Group Jun 2022 – Sep 2022

- Designed UAV payload with software-defined radios to validate multipath channel model for characterization of lunar terrain
- Collected data and verified testbed measurement precision through Doppler effect signal processing in MATLAB

PROJECTS

Low-Jitter 8 GHz Delay-Locked Loop (DLL) in 45nm CMOS Mar 2025

- Designed and simulated a 45nm DLL to align a noisy input signal with a clean reference clock
- Implemented phase detector, loop filter, and delay line, optimizing for jitter, power, and duty-cycle distortion
- Verified locking behavior and performance through closed-loop simulations and jitter analysis under noise conditions

Pipelined CORDIC Calculator with JTAG Interface Feb 2025

- Implemented a 16-bit fixed-point (Q1.14) CORDIC calculator in VHDL, supporting trigonometric and hyperbolic functions
- Optimized performance through a configurable pipeline depth for faster computation and throughput with a Xilinx FPGA
- Integrated JTAG interface for real-time debugging and system validation

AT-AT Bluetooth Robot (Caltech EE 110abc) Jun 2024

- Designed two custom PCBs for a 12-DOF walking robot, integrating servo motors, IMUs, keypads, LCDs, laser diodes, and Bluetooth antenna design, supporting a network of three robot controllers and one remote using a TI microcontroller
- Wrote software in ARM assembly for device drivers and timing-critical functions, and developed software in C for TI RTOS, managing the four-device BLE network and all other system functionalities

ADDITIONAL

Activities: FIRST Robotics (2017-2021), Caltech FSAE (2022-2024), Caltech NCAA Baseball (2021-2025)
Programming Languages: Verilog, VHDL, Python, C, C++, MATLAB, ARM/x86 Assembly, Unix, Tcl
Technical Proficiencies: Embedded Systems, RTL Design, VLSI Physical Design, Digital and Analog Circuit Design
Certifications: Cadence RTL-to-GDSII Flow, Cadence Digital IC Design Fundamentals, Cadence Static Timing Analysis
Misc. Awards: Eagle Scout (2019), Academic All-District NCAA Baseball (2023)